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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/788,777	02/27/2004	Brian M. Collins	884.961US2	6145

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EXAMINER	
CHOI, WOO H	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 02/17/2005 .

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/788,777	COLLINS ET AL.	
	Examiner	Art Unit	
	Woo H. Choi	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,8-10,12-18,21-26,29-34,37 and 38* is/are rejected.

7)☐ Claim(s) *6,7,11-13,19,20,27,28,35 and 36* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/27/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 3, 4, 14, 16, 17 and 18 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

3. With respect to claims 3, 4, 17, and 18, each of the claims recites the limitation "a number of" registers. A number can be interpreted as any number, which would include zero in which case the claims do not further limit their parent claims. Also, one of the ordinary definitions of "a number" is many, which denotes an indefinite quantity.

4. Claim 14, recites the limitation "the allocation of memory" in line 6, page 14. There is insufficient antecedent basis for this limitation in the claim.

5. Claim 16 recites the limitation "the physical address" in line 17, page 14. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1 – 5, 8 – 10, 14 – 18, 21 – 26, 29 – 34, and 37 – 38 are rejected under 35 U.S.C. 102(e) as being anticipated by Garcia *et al.* (US Patent No. 6,163,834, hereinafter "Garcia").

8. With respect to claims 1, 15, 16, 23 and 31, Garcia discloses a system comprising:

an operating system (operating system is inherent in an operating computer system, see also col. 1, lines 32 – 34 and figure 1);

a system memory (col. 2, lines 12 – 22); and

a channel adapter (Network Interface Controller, NIC and associated address translation tables) operatively coupled to the operating system (figure 1), wherein the channel adapter includes comparison logic (figure 5) to determine which segment (figure 7, TPT entry) of multiple segments of a block (figures 5 and 7, TPT 56) of memory in the system memory is being addressed by a received index (figure 5, Memory Handle Index/Virtual Address) and to generate the physical address (PSA) of the location in the block of memory for the received index, the comparison logic adapted to compensate for the block of memory having a segment that is non-contiguous with the other segments of the block of memory to access the block of

memory as a single contiguous block of memory (see figures 8A – 8B, non contiguous segments or entries are rearranged into a contiguous block by reassigning memory handles).

9. With respect to claim 2, the comparison logic is adapted to compensate for a segment of the block of memory being expandable (col. 2, lines 39 – 42).

10. With respect to claims 3, 4, 17, 18, 25 and 33, the channel adapter further includes:

a number (figure 6, MHT 54) of first registers (figure 6, TPT Ext 63), each first register to contain a value denoting a size of a corresponding segment of the multiple segments of the block of memory (figure 6, the Extent field contains the number of consecutive 4K byte pages for this TPT block); and

a number of second registers (TPT Start 62), each of the second registers to contain a value denoting a starting physical address of an associated segment of the multiple segments of the block of memory (TPT Start field contains the starting, or base, address of the TPT entries).

11. With respect to claim 5, the apparatus further includes a comparator responsive to the number of first registers to perform an out of bounds check (figure 5, TPT Extent Violation logic).

12. With respect to claim 9, the comparison logic further includes a detector to provide an error signal indicating an attempt to access a segment that is currently not enabled (figure 5, Memory Handle Table size violation).

13. With respect to claim 10, the number of first registers is one first register (54 includes one register) to contain the value denoting the size of each segment of the multiple segments, the multiple segments having the same size (figure 7, entries pointed to AH4 and AH4 are of the same size, one entry, and the size of all of the entries in the TPT are the same).

14. With respect to claim 14, the comparison logic is adapted to compensate for the allocation of memory for the segments of the block of memory by an operating system in response to a request by an application (figure 1 and col. 1, lines 27 – col. 2, lines 18).

15. With respect to claim 22, the channel adapter is a target channel adapter (see rejection of claim 16 above, TCA is merely another name for the channel adapter of claim 16, which presumably changes depending on where it is used, see specification, page 1, lines 20 – 21).

16. With respect to claims 24 and 32, the method further includes dynamically allocating memory to a segment of the block of memory (col. 5, lines 46 – 49, TPT memory locations are allocated for new entries, i.e. segments, for newly registered memory regions).

17. With respect to claims 9, 29, 30, 37 and 38, the method further includes disabling a segment of the multiple segments of the block of memory (figure 6, V valid bit); and

detecting an attempt to access a segment that is disabled and providing error signal indicating the attempted access to the disabled segment (in figure 6 Garcia disclose that protection fails if this bit is clean).

18. With respect to claims 8, 21, the comparison logic further includes an enable register, the enable register containing a bit for each of the multiple segments of the block of memory, each bit denoting whether the associated segment of the multiple segments of the block of memory is enabled, the enable register being software programmable (figure 6, Valid bit, see also col. 4, lines 63 – 67, unused entries, or "disabled" entries are marked as invalid).

19. With respect to claims 26 and 34, generating a physical address of the location in the block of memory for the received index includes generating the physical address by adding the received index to a base address (figure 5, memory handle base MHB is added to the memory handle index MHI to generate the physical address).

Allowable Subject Matter

20. Claims 6, 7, 11 – 13, 19, 20, 27, 28, 35 and 36, are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims and if the deficiencies of their respective parent claims under 35 USC 112, second paragraph, are corrected.

Conclusion

21. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Teitenberg et al. (US Patent No. 6,421,769) disclose another channel adapter with address translation and protection logic that use non-contiguous memory segments, base addresses and segment sizes. Berry (US Patent Application Publication No. 2002/0078271) discloses TPT that uses base addresses and segment sizes. Khaladi et al. (US Patent No.5,784,707) and Horan et al. (US Patent No. 5,999,198) address translation logics adapted to compensate for blocks of memory having segments that are non-contiguous to access the blocks as contiguous blocks.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Woo H. Choi whose telephone number is (571) 272-4179. The examiner can normally be reached on M-F, 9:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (571) 272-4182. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Woo H. Choi
February 14, 2005